REMARKS

In the Office Action, the Examiner noted that claims 1, 2, and 4-13 are pending in the application, and that claims 1, 2, and 4-13 are rejected. By this response, claim 1 is amended to include the limitations of claims 7 and 12. Claims 3, 7, 12, and 13 are canceled without prejudice. New claim 14 is added. In view of the above amendments and the following discussion, the Applicant submits that none of the claims now pending in the application are obvious under the provisions of 35 U.S.C. § 103. Thus, the Applicant believes that all of these claims are now in condition for allowance.

I. REJECTION OF CLAIMS UNDER 35 U.S.C. § 112

The Examiner rejected claim 13 under 35 U.S.C. 112, second paragraph, as lacking antecedent basis for the limitation "the overetch step." Claim 13 is canceled by this response, thus obviating the rejection.

The Examiner rejected claims 11-13 under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. Specifically, the Examiner stated that "Applicant has not shown where in the specification describes the etching is carried out in the absence of oxygen, and the pulsed bias power is applied during the overetch step." Claims 12 and 13 are canceled by this response. As such, the rejection to claims 12 and 13 are moot. The limitations of claim 11 are shown in the Application at least at page 3, lines 22-24. Thus, Applicants submit that claim 11 fully satisfies the requirements of 35 U.S.C. § 112.

II. REJECTION OF CLAIMS UNDER 35 U.S.C. §102(b)

The Examiner rejected claims 1 and 5 as being anticipated by Savas (United States patent 5,938,828, issued November 16, 1999). The rejection is respectfully traversed.

More specifically, the Examiner alleged that "Savas describes a method for etching silicon comprising: anisotropically etching openings in silicon with sulfur hexafluoride etchant...in a plasma etching chamber with a powered substrate support while pulsed bias power is applied to the substrate support electrode during the etch

step..." (Office Action, Section 2, ¶1). The Examiner concluded that Savas anticipates Applicants' invention as recited in claim 1. Applicants respectfully disagree.

Savas teaches that "a strong bias is applied to the substrate in short bursts. Preferably, multiple burst occur during the average transit time for an ion to cross the plasma sheath and reach the substrate surface. Ions are pulsed toward the surface for etching." (Abstract, lines 17-21) Savas is devoid of any teaching or suggestion of overetching.

In view of the forgoing, Savas does not teach or suggest each and every element of Applicants' invention as recited in claim 1. Namely, Savas does not teach or suggest "overetching the silicon while applying pulsed bias power to the substrate support electrode" as recited in claim 1. Therefore, claim 1 is not anticipated by Savas. Claims 2, 4-6, 8-11, and 14 are patentable over Savas at least by virtue of their dependence from claim 1.

III. REJECTION OF CLAIMS UNDER 35 U.S.C. §102(e)

The Examiner rejected claims 1, 6, and 8-10 as being anticipated by Wang (United States patent 6,593,244, issued July 15, 2003). The rejection is respectfully traversed.

More specifically, the Examiner alleged that "Wang describes a method for etching silicon comprising: anisotropically etching openings in silicon with sulfur hexafluoride etchant...in a plasma etching chamber with a powered substrate support while pulsed bias power is applied to the substrate support electrode during the etch step..." (Office Action, Section 3, ¶1). The Examiner concluded that Wang anticipates Applicants' invention as recited in claim 1. Applicants respectfully disagree.

Wang teaches that "Preferably the bias power to the cathode electrode is pulsed for a period of from 1 microsecond up to 900 milliseconds, and at duty cycles of from about 10 to 99%, to reduce charge-induced defects, such as notching, at or close to a conductor/insulator interface or a conductor/photoresist interface, for example. In particular, notching of silicon on insulator at the silicon-insulator interface can be greatly

reduced using pulsed bias power during the etch step." (column 3, lines 32-39) Wang is devoid of any teaching or suggestion of overetching.

In view of the forgoing, Wang does not teach or suggest each and every element of Applicants' invention as recited in claim 1. Namely, Wang does not teach or suggest "overetching the silicon while applying pulsed bias power to the substrate support electrode" as recited in claim 1. Therefore, claim 1 is not anticipated by Wang. Claims 2, 4-6, 8-11, and 14 are patentable over Wang at least by virtue of their dependence from claim 1.

IV. REJECTION OF CLAIMS UNDER 35 U.S.C. §103(a)

Rejection in view of Savas

The Examiner rejected claims 2 and 4 as being unpatentable over Savas. As noted above, Savas does not anticipate or suggest claim 1. Thus Applicant believes, claims 2 and 4 are patentable over Savas for the same reasons claim 1 is patentable over Savas.

Rejection in view of Savas and admitted prior art

The Examiner rejected claims 6-11 as being unpatentable over Savas in view of admitted prior art. As noted above, Savas does not anticipate or suggest claim 1. It is respectfully submitted that the combination of Savas and admitted prior art does not teach, suggest, or render obvious claim 1, e.g., Savas does not teach overetching.

More specifically, the Examiner conceded that "Savas doesn't describe a deposition step prior to the etching step using a pressure of 5-300 mtorr and no bias power and overetch deposition and overetch steps are carried out after the etching step." (Office Action, Section 6, ¶2). The Examiner alleged, however, that "Admitted prior art teaches a conventional method of etching silicon comprising a deposition step prior to etching step using a pressure of 18 mtorr and overetch deposition and overetch steps are carried out after the etching step. There is no bias power applied during the deposition step and the overetch step would remove any debris from the bottom of the

opening." As such, the Examiner concluded that "it would have been obvious for one skill in the art to modify Savas in light of admitted prior art because it teaches the other steps of a conventional etching method for silicon where the deposition would protect the photoresist pattern." Applicants respectfully disagree.

As stated previously, Savas teaches that "a strong bias is applied to the substrate in short bursts. Preferably, multiple burst occur during the average transit time for an ion to cross the plasma sheath and reach the substrate surface. Ions are pulsed toward the surface for etching." (Abstract, lines 17-21).

Admitted prior art teaches "The overetch step was then carried out using 9 watts of bias power..." (Application, page 2, lines 17-18)

Applicants' claim 1 recites:

> "A method of reducing notching in etched anisotropic openings in silicon over an insulator layer comprising:
> anisotropically etching openings in silicon with a sulfur hexafluoride etchant in a plasma etch chamber fitted with a powered substrate support while applying pulsed bias power to the substrate support electrode during the etch step;
>
> overetching the silicon while applying pulsed bias power to the substrate support electrode." (emphasis added)

Savas teaches that a pulsed bias power is applied to the substrate during an etch step. Admitted prior art teaches that bias power is applied to the substrate during an overetch step. However, neither the admitted prior art nor Savas teach using a pulsed bias power during an overetch step. Thus, any combination of the admitted prior art and Savas would lack such a teaching. Therefore, Applicants contend that claim 1 is patentable over Savas in view of admitted prior art and, as such, fully satisfies the requirements of 35 U.S.C. §103.

Furthermore, claims 2, 4-6, 8-11, and 14 depend, either directly or indirectly, from claim 1 and recite additional features therefor. Since the combination of Savas and admitted prior art would not produce Applicants' invention as recited in claim 1, dependent claims 2, 4-6, 8-11, and 14 are also not obvious and are allowable.

Rejection in view of Wang and admitted prior art

The Examiner rejected claims 7, 12, and 13 as being unpatentable over Wang in view of admitted prior art. Claims 7, 12, and 13 have been canceled and their limitations have been incorporated into claim 1. As such, the following response will be addressed to claim 1. Wang cannot be properly cited as prior art under 35 U.S.C. 103. Under 35 U.S.C. 103(c), "Subject matter developed by another person, which qualifies as prior art only under one or more of subsections (e), (f), and (g) of section 102 of this title, shall not preclude patentability under this section where the subject matter and the claimed invention were, at the time the invention was made, owned by the same person or subject to an obligation of assignment to the same person." Since Wang and the claimed invention were subject to an obligation of assignment to the same person (Applied Materials) at the time the inventions were made, Wang may not be properly used as prior art under 35 U.S.C. 103. Therefore, it is respectfully submitted that Wang was improperly cited as art under 35 U.S.C. 103.

IV. DOUBLE PATENTING REJECTION

The Examiner rejected claims 1, 2, 4, and 5 as being unpatentable over claims 1, 6-9, 11, and 12 of Wang in view of Savas. The Examiner also rejected claims 6-13 as being unpatentable over claims 1, 6-9, 11, and 12 of Wang in view of Savas and further in view of admitted prior art.

The combination of Wang and Savas does not anticipate, suggest, or render obvious claim 1, as amended. Claims 1, 6-9, 11, and 12 of Wang fail to recite an overetch step. Savas teaches that "a strong bias is applied to the substrate in short bursts. Preferably, multiple burst occur during the average transit time for an ion to cross the plasma sheath and reach the substrate surface. Ions are pulsed toward the surface for etching." (Abstract, lines 17-21) Savas is devoid of any teaching or suggestion of overetching. Claims 1, 6-9, 11, and 12 of Wang and Savas fail to alone, or in combination, recite all of the elements of claim 1. Furthermore, neither Wang nor Savas provide a suggestion for overetching. Thus, claim 1 is patentable over Wang in

view of Savas. Claims 2, 4-6, 8-11, and 14 are allowable at least by virtue of their dependence from claim 1.

The combination of admitted prior art to Savas and claims 1, 6-9, 11, and 12 of Wang also fails to render claim 1 obvious. Admitted prior art teaches "The overetch step was then carried out using 9 watts of bias power..." (Application, page 2, lines 17-18) However, the admitted prior art fails to teach overetching the silicon while applying pulsed bias power to the substrate support electrode as recited in amended claim 1. Thus, claim 1 is patentable over Wang in view of Savas. Claims 2, 4-6, 8-11, and 14 are allowable at least by virtue of their dependence from claim 1.

CONCLUSION

Thus, Applicants submit that none of the claims presently in the application are indefinite under the provisions of 35 U.S.C. § 112, or obvious under the provisions of 35 U.S.C. § 103. Consequently, Applicants believe that all these claims are presently in condition for allowance. Accordingly, both reconsideration of this application and its swift passage to issue are earnestly solicited.

If, however, the Examiner believes that there are any unresolved issues requiring adverse final action in any of the claims now pending in the application, it is requested that the Examiner telephone Mr. Raymond R Moser Jr., Esq. at (732) 530-9404 so that appropriate arrangements can be made for resolving such issues as expeditiously as possible.

Respectfully submitted,

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